TOYOTA FLD 19Fver3 - Task #1736

Task # 1610 (进行中): FLD System Architecture Design

Task # 1612 (进行中): FLD_SWEA: Software Achitechture Design

Task # 1710 (进行中): FLD_SWEA: Software Achitechture Design - Software Components

Task # 1720 (进行中): FLD_SWEA: Software Achitechture Design - Software Middle Layer Components

FLD_SWEA: Software Achitechture Design - Enviroment Signal Processing

2023-10-25 18:28 - 德乐 秦

状态:	进行中	**开始日期:**	2023-12-07
优先级:	普通	**计划完成日期:**	2023-12-09
指派给:	德乐 秦	**% 完成:**	0%
类别:		**预期时间:**	0.00 小时
目标版本:	FLD_H000.1_A001.00.00	**耗时:**	0.00 小时

描述

1. Left Right Detection
2. board Temperature conversion
3. Vechile voltage conversion
4. LB/TURN triggle signal